

WHAT IS CLAIMED IS:

1. A plurality of chip devices comprising:
  - 2 a plurality of bottom leadframes each including a plurality of leads;
  - 3 a plurality of bumped dies, each bumped die being on a corresponding bottom leadframe and including a source and gate solder bump array;
  - 4 a plurality of top leadframes, each top leadframe being coupled to a corresponding bumped die and including a plurality of leads; and
  - 5 four rails, a first rail being connected to a first side of each of the top leadframes, a second rail being connected to a second side of each of the top leadframes, a third rail being connected to a first side of each of the bottom leadframes, and a fourth rail being connected to a second side of each of the bottom leadframes;
  - 6 wherein each bottom leadframe has leads coupled to drain terminals on its corresponding bumped die;
  - 7 wherein each top leadframe has a lead coupled to a gate terminal on its corresponding bumped die and leads coupled to source terminals on its corresponding die;
  - 8 and
  - 9 wherein the first rail is coupled to the third rail and the second rail is
  - 10 coupled to the fourth rail.
1. An arrangement in accordance with claim 1 wherein the solder bumps consist of one of Pb-Sn, Pb-Sn-Ag or Sn-Sb.
1. An arrangement in accordance with claim 1 wherein the leads are coupled to the gate terminal and the source terminals via pads.
1. An arrangement in accordance with claim 1 further comprising a plurality of molded bodies, each body encapsulating a portion of a corresponding top leadframe and a corresponding bottom leadframe, and a corresponding bumped die therebetween.
1. An arrangement in accordance with claim 1 wherein the chip devices are DMOS devices.

1                   6.       An arrangement in accordance with claim 1 wherein the top  
2   leadframes include slots defined therein.

1                   7.       A method of making a chip device, the method comprising:  
2                   providing a plurality of bottom leadframes coupled to one another with a  
3                   pair of rails;  
4                   attaching a corresponding bumped die including a source and gate solder  
5                   bump array to each bottom leadframe;  
6                   providing a plurality of top leadframes coupled to one another with a pair  
7                   of rails; and  
8                   flipping the plurality of top leadframes such that each top leadframe  
9                   contacts the solder bumps on a corresponding bumped die.,

1                   8.       A method in accordance with claim 7 further comprising placing a  
2                   molded body around each top and bottom leadframe with a corresponding bumped die  
3                   therebetween.

1                   9.       A method in accordance with claim 7 further comprising spot  
2                   welding a rail of the bottom leadframe and a rail of the top leadframe together.

1                   10.      A method in accordance with claim 9 further comprising reflowing  
2                   the solder bumps.

1                   11.      A method in accordance with claim 7 further comprising  
2                   pressfitting a rail of the bottom leadframe and a rail of the top leadframe together.

1                   12.      A method in accordance with claim 11 further comprising  
2                   reflowing the solder bumps.

1                   13.      A method in accordance with claim 7 wherein the bumped die is  
2                   attached to the bottom leadframe with an adhesive, the adhesive being cured sometime  
3                   during the method after the die is attached thereto.

1                   14.     A method in accordance with claim 7 wherein the bumped die is  
2     attached to the bottom leadframe with soft solder.

1                   15.     A method of making a plurality of chip devices, the method  
2     comprising:  
3                   providing a plurality of top leadframes coupled to one another with a pair  
4     of rails;  
5                   flipping a bumped die including a source and gate solder bump array on  
6     each top leadframe such that each bumped die contacts the gate and source pads of  
7     topframe; and  
8                   providing a plurality of bottom leadframes being coupled to one another  
9     with a pair of rails;  
10                  flipping the top leadframes onto the plurality of bottom leadframes such  
11     that a bumped die is between each top leadframe and a corresponding bottom leadframe.

1                   16.     A method in accordance with claim 15 further comprising placing a  
2     molded body around each top and bottom leadframe with a corresponding bumped die  
3     therebetween.

1                   17.     A method in accordance with claim 15 further comprising spot  
2     welding a rail of the bottom leadframe and a rail of the top leadframe together.

1                   18.     A method in accordance with claim 17 further comprising  
2     reflowing the solder bumps.

1                   19.     A method in accordance with claim 15 further comprising  
2     pressfitting a rail of the bottom leadframe and a rail of the top leadframe together.

1                   20.     A method in accordance with claim 19 further comprising  
2     reflowing the solder bumps.

1                   21.     A method in accordance with claim 15 wherein the die is attached  
2     to the bottom leadframe with soft solder.

1                   22.     A method in accordance with claim 15 wherein the die is attached  
2     to the bottom leadframe with an adhesive, the adhesive being cured sometime during the  
3     method after the die is attached thereto.

1                   23.     A method of making a plurality of chip devices, the method  
2     comprising:  
3                   providing a plurality of top leadframes coupled to one another with a pair  
4     of rails;  
5                   providing a plurality of bottom leadframes coupled to one another with a  
6     pair of rails, each bottom leadframe including a die attach pad;  
7                   placing a bumped die including a source and gate array on each die attach  
8     pad of each bottom leadframe; and  
9                   coupling the top and bottom leadframe rails together such that each  
10    bumped die contacts the solder bumps of a corresponding top leadframe.

1                   24.     A method in accordance with claim 23 further comprising placing a  
2     molded body around each top and bottom leadframe with a corresponding bumped die  
3     therebetween.

1                   25.     A method in accordance with claim 23 further comprising spot  
2     welding the rails of the bottom leadframe and the rails of the top leadframe together.

1                   26.     A method in accordance with claim 25 further comprising  
2     reflowing the solder bumps.

1                   27.     A method in accordance with claim 23 further comprising  
2     pressfitting the rails of the bottom leadframe and the rails of the top leadframe together.

1                   28.     A method in accordance with claim 27 further comprising  
2     reflowing the solder bumps.

1                   29.     A method in accordance with claim 23 wherein each bumped die is  
2     attached to the bottom leadframe with an adhesive, the adhesive being cured sometime  
3     during the method after the die is attached thereto.

1                           30.     A method in accordance with claim 23 wherein each bumped die is  
2     attached to the bottom leadframe with soft solder.

Add  
at